(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 425 194 A2**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: **90311409.8**

(51) Int. Cl.5: **G06F 13/362**

(22) Date of filing: **17.10.90**

(30) Priority: **23.10.89 US 425765**

(43) Date of publication of application:
**02.05.91 Bulletin 91/18**

(84) Designated Contracting States:
**DE FR GB**

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## (54) Computer system.

(57) A logic controlled delay circuit (305) is connected into the arbitration logic (155) of a computer system of the type having a main data bus (115) which is subject to control by multiple masters (140). The delay is so programmed that the default master, which is the main processor (CPU) (100) for the system and is assigned the residual or default priority, is assured a predefined portion of the time available on the bus (115). By so inserting and controlling the delay that the "hold" signal to the CPU (100) is delayed whenever the CPU (100) is granted access to the bus (115) , other devices, are unable to seize the bus (115) until the delay has ended at which time the CPU (100) is triggered by the delayed signal to respond with an acknowledge which serves to permit arbitration to begin. By this technique a standard microprocessor such as an Intel 80386 can operate in such an architecture without being preempted from the bus (115) by the higher priority devices (140) to an extent that system operation deteriorates.

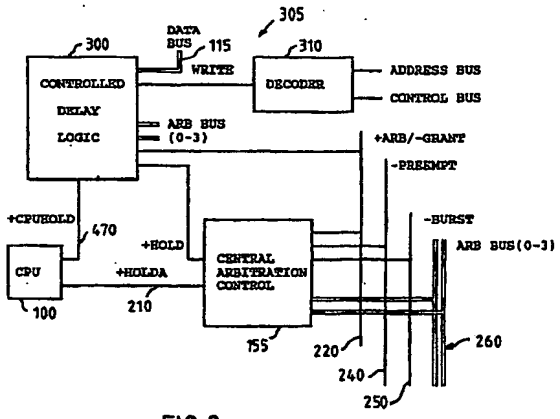



FIG. 3

# COMPUTER SYSTEM

The present invention relates in general to a computer system and in particular to a computer system for enabling a plurality of devices to manage data transfers over a main data bus with priority levels being established to ration time on the bus.

Computer systems such as those having a Micro Channel architecture (microchannel is a trademark of IBM Corporation), have multiple masters which can each manage data transfers over the main data bus of the system. Such masters can relieve the main processing unit (CPU) from detailed involvement in data transfers between input /output (I/O) devices and main memory and also between I/O devices. By offloading these duties the CPU is permitted to more fully concentrate its efforts on processing data and setting up transfers that other devices will execute.

In such systems, priorities are established for the respective devices on the data bus to allocate bus time. The CPU is assigned the default or residual priority recognising that the main work on the bus is desirably allocated to other devices. If a queue develops the devices including the CPU vie for the bus during each arbitration cycle and the highest in priority wins. As burst devices may continually assert a high priority, a "fairness" limitation is often used with the burst devices to force them to wait until the existing queue disappears before they may reenter the queue.

This process works well to efficiently allocate bus time unless the duty on the data bus becomes high. In that case, the CPU gets a chance on the bus infrequently, as the priority scheme permits, and then gets "bumped off" after one bus cycle if another device preempts. This situation can "lock out" the CPU to an extent that it cannot perform the preparatory setup needed for data transfers or other activity such as memory access that it requires to perform tasks. when this condition is reached the overall system performance deteriorates and, in an extreme case, there may be a system crash.

An aim of the present invention is therefore to provide the CPU of such a system with a preselected amount of time on the data bus even during high duty cycle periods for data transfer.

In accordance with the present invention, there is now provided a computer system comprising a main processor having a terminate input responsive to a terminate signal for setting the processor to an inactive state, arbitration logic for connecting a main data bus to one of a plurality of master devices in response to a bus request signal and in accordance with predefined priority levels associated with the master devices wherein the processor is assigned a default priority level, characterised in that the system further comprises a preempt de lay circuit including: detector logic for generating a selection signal in response to the arbitration logic selecting the processor, and delay logic connected between the arbitration logic and the terminate input for extending a period for which the processor is connected to the main data bus by a predetermined time upon receiving the selection signal.

Viewing the present invention from a second aspect, there is now provided, in a computer system having a main processor which can be driven to an inactive state by a terminate signal and a main data bus which is allocated by arbitration logic which repeatedly selects a bus owner according to predefined priority levels as bus requests arrive among plural master devices including the main processor which is assigned the default priority level, a preempt delay circuit comprising: detector logic which creates a selection signal whenever the arbitration logic selects the main processor and delay logic connected to delay signals in a path extending from the arbitration logic device and the terminate input of the main processor.

In an example of the present invention to be described later, there is provided a computer system in which the response to a preempt is modified in the event of the CPU having s ownership of the data bus. The modification is achieved by introducing a logic controlled delay into signal lines between the arbiter and the CPU. The delay is provided without restructuring the arbitration process of the system. Furthermore, the delay is provided without changing the control bus of the system or requiring a different microprocessor such as a microprocessor with an expanded command set.

An embodiment of the present invention will now be described by way of example only with reference to the accompanying drawings in which:

Figure 1 is a block diagram of a system suitable for implementing the invention;

Figure 2 is a block diagram of a prior art signal connection between a central arbitration controller and a CPU of a system with priority arbitration;

Figure 3 is a block diagram indicating modifications to signals passed from the arbitration controller to the CPU in accordance with the present invention.

Figure 4 is a block diagram of an electrical circuit of the present invention.

Figure 5 is a timing diagram illustrating control signals for a prior art system of the kind indicated in Figure 2;

Figure 6 is a timing diagram illustrating control signals in accordance with the present invention.

A presently preferred implementation for the invention will now be described in detail with reference to the drawings. Referring to Figure 1 a preferred system for implementing the invention includes a CPU 100, such as an Intel Corporation 80386 microprocessor, which is connected to other system elements over a set 105 of system signal busses including a control bus 110, a data bus 115 and an address bus 120. Connected to the bus set 105 are a read only memory (ROM) 125 which retains permanently resident system logic, a main memory 130, which is directly addressable read/write storage, and a memory controller 135.

In a system according to the present invention there is preferably provided a connection point 140 permitting bus interface devices 140 such as bus master devices which can control a data bus to be connected to the system bus set 105. These connections are usually made by inserting circuit boards into slots fitted with card edge connectors (indicated in edge view only in Figure 1). The interface devices 145 may connect to a variety of other devices such as input/output (I/O) devices 150. Such devices 150 may include, for example disc drives or tape units (not shown). Such a system arrangement including interface devices 145 which may be bus masters and control the data bus 115 is specified for a Micro Channel architecture (microchannel is a trademark of IBM Corporation) described in detail in an IBM Corporation Manual entitled "personal System/2 Hardware Interface Technical Reference 68X2330". With such a system, a central arbitration controller 155 establishes the priority of devices taking control of the data bus 115 and a DMA controller 160 coordinates the actual transfers over such bus as is well known. A typical set of arbitration priority level assignments is illustrated at Table 1.

TABLE 1

| ARBITRATION LEVEL | PRIMARY ASSIGNMENT |
|---|---|
| -2 | MEMORY REFRESH |
| -1 | ERROR RECOVERY |
| 0 | DMA Port 0 |
| 1 | DMA Port 1 |
| 2 | DMA Port 2 |
| 3 | DMA Port 3 |
| 4 | DMA Port 4 |
| 5 | DMA Port 5 |
| 6 | DMA Port 6 |
| 7 | SPARE |
| 8 | SPARE |
| 9 | SPARE |
| A | SPARE |
| B | SPARE |
| C | SPARE |
| D | SPARE |
| E | SPARE |
| F | SYSTEM BOARD PROCESSOR (CPU) |

Referring now to Figure 2, the prior art includes a path 200 providing a connection between the central arbitration control 155 and the CPU 100 to carry a terminate operation signal ("HOLD") at the pin (not shown) corresponding to that signal input for the particular processor that is employed as the CPU. A path

210 is, moreover, provided to carry an acknowledge signal back to the arbitration control 155. Also indicated are channels of the control bus 110 (see Figure 1) which serve in allocating the data bus 115.

A channel 220 carries a +ARB/-GRANT signal that serves to separate periods when arbitration to establish bus ownership is occurring (ARB) and periods when ownership is fixed (GRANT) and the various masters 230 can function respective of that ownership assignment. A channel 240 serves to carry a signal -PREEMPT which indicates when one or more master devices,such as device 240 and including the CPU 100 are waiting to access the data bus 115. A channel 250 carries the -BURST signal which is asserted by a device 240 when it owns the data bus 115 to indicate whether it is a device capable of multiple or burst transfers.

Also connected to the central arbitration control 155 is an arbitration bus 260 consisting of preferably four lines (0-3) on which arbitration levels are asserted to achieve ownership of the data bus 115 and then, during the time GRANT is asserted on channel 220, to identify the owner.

Now referring to Figure 3, the signal path 200′ is directed to a logic circuit 300 of a complex 305 which according to the present invention inserts a delay and creates a modification to the HOLD signal to result in a signal +CPUHOLD which is applied at the terminate operation input point for the CPU 100. For an Intel Corporation 80386 this would be the "HOLD" pin of the PGA module. A decoder 310 provides a WRITE signal to the logic circuit 300 over line 320. It is applied to write new delay duration information into a register 400 (see Figure 4) which is supplied to a timer 410 over a bus 420.

Continuing with Figure 4, an AND gate 430 is connected to receive the inverse of the +HOLD signal on line 200, the inverse of the +ARB/-GRANT signal on line 220 and the bus owner information on ARB bus 260. The output of the AND gate 430 is a signal +CPUSEL on line 440 which is applied to timer 410 to trigger a timeout for the period specified on bus 420. The signal +CPUSEL triggers the timeout signal +DELAY on line 450 in those situations when a terminate request is sent from the arbitration control and the CPU 100 owns the DATA bus 115 (-GRANT is active and the arbitration level is 1111, hexadecimal F as indicated in Table 1 to identify the CPU). The signal +HOLD of line 200′ and the inverse of the signal DELAY are applied to an AND gate 460 to produce the signal +CPUHOLD on la line 470 which applies that signal to the CPU 100 (see Figure 3). The effect of this modification of the termination signal +HOLD is readily seen by comparing the illustrative prior art timing diagram of Figure 5 with the illustrative timing diagram for the preferred implementation of Figure 6. As is indicated the CPU 100 may remain owner of the data bus 115 until the delay period expires.

The present invention has been described in detail with reference to a presently preferred embodiment thereof. It will however be appreciated that various alternatives within the scope of the present invention will be suggested to those skilled in the art and in determining the scope for the present invention reference should be made to the claims considering any equivalents to which applicant is entitled.

## Claims

1. A computer system comprising a main processor (100) having a terminate input (200) responsive to a terminate signal for setting to the processor (100),
arbitration logic (155) for connecting a main data bus (115) to one of a plurality of master devices (140) in response to a bus request signal and in accordance with predefined priority levels associated with the master devices (140) wherein the processor (100) is assigned a default priority level,
characterised in that the system further comprises a preempt delay circuit (305) including:
detector logic (430) for generating a selection signal in response to the arbitration logic (155) selecting the processor,
and delay logic (410,460) connected between the arbitration logic (155) and the terminate input (200) for extending a period for which the processor (100) is connected to the main data bus (115) by a predetermined time upon receiving the selection signal.

2. A computer system as claimed in claim 1 wherein the delay circuit (305) further comprises a register (400) for storing the predetermined time.

3. A computer system as claimed in claim 2 wherein the delay circuit (305) further comprises a decoder (310) for generating a write signal connected to the register (400) for enabling the predetermined time stored in the register (400) to be revised.

4. A computer system as claimed in any preceding claim wherein the delay logic (410,460) comprises a timer (410) triggered by the selection signal for generating a timeout signal in response to the Predetermined time elapsing.

5. A computer system as claimed in claim 4 wherein the delay logic further comprises an AND gate (460)

for generating the terminate signal in response to the timeout signal and a hold signal in combination.

6. A computer system as claimed in any preceding claim wherein the detector logic (430) comprises an AND gate (430) having inputs connected to the arbitration logic (155).

7. A computer system as claimed in any preceding claim wherein the processor (100) is an 80386 processor.

8. In or for a computer system having a main processor (100) which can be driven to an inactive state by a terminate signal and a main data bus (115) which is allocated by arbitration logic (155) which repeatedly selects a bus owner according to predefined priority levels as bus requests arrive among plural master devices (140) including the main processor which is assigned the default priority level, a preempt delay circuit (305) comprising:

detector logic (430) which creates a selection signal whenever the arbitration logic (155) selects the main processor (100) and

delay logic (410,460) connected to delay signals in a path extending from the arbitration logic (155) and the terminate input (200) of the main processor.

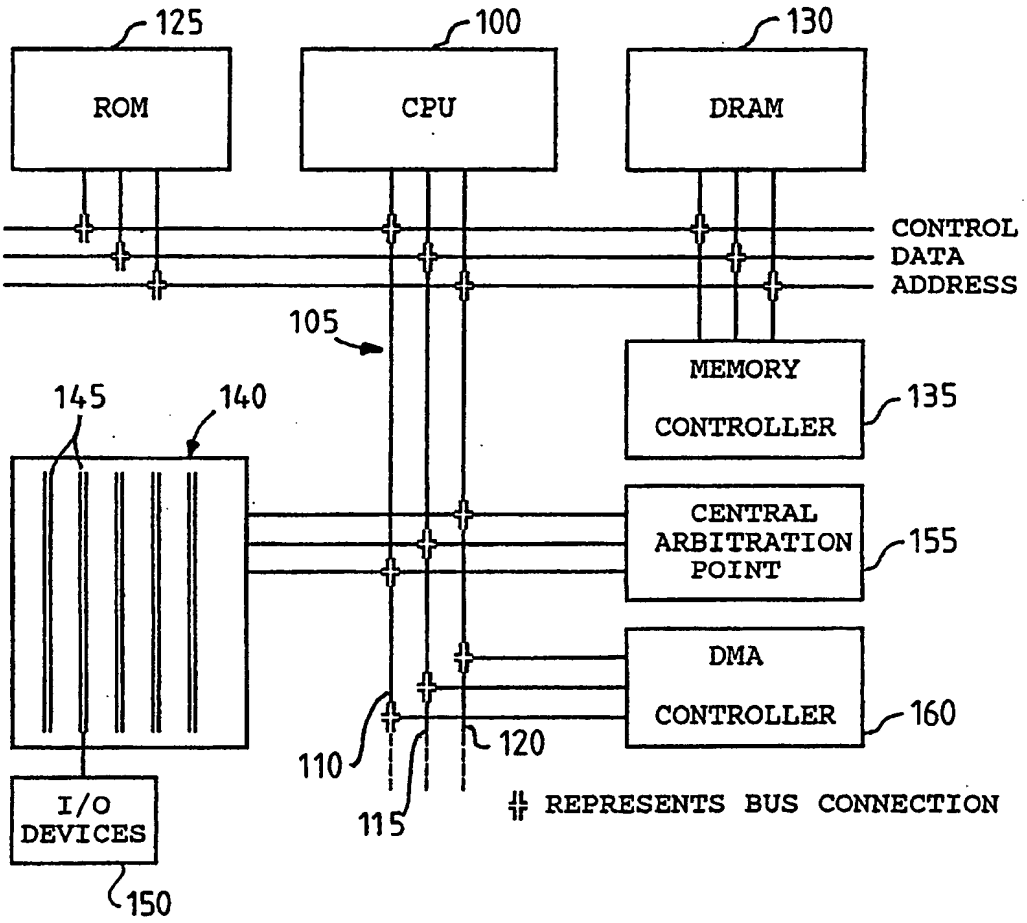

125
ROM
100
CPU
130
DRAM
CONTROL
DATA
ADDRESS
105
MEMORY
CONTROLLER
135
145
140
CENTRAL
ARBITRATION
POINT
155
DMA
CONTROLLER
160
110
120
115
I/O
DEVICES
150
# REPRESENTS BUS CONNECTION

FIG. 1

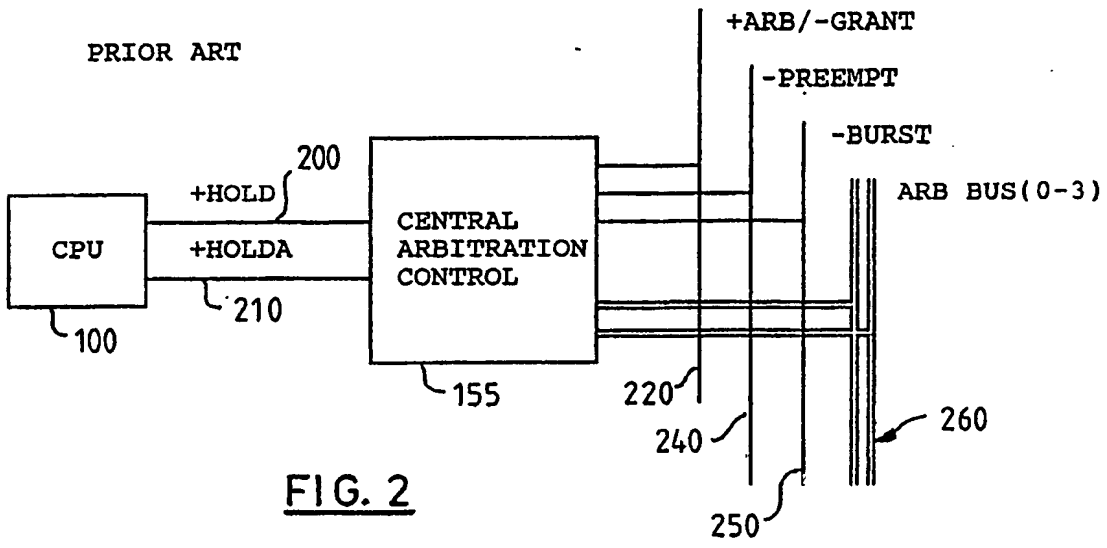

PRIOR ART
+ARB/-GRANT
-PREEMPT
-BURST
ARB BUS(0-3)
200
+HOLD
CPU
+HOLDA
CENTRAL
ARBITRATION
CONTROL
210
100
155
220
240
260
250

FIG. 2

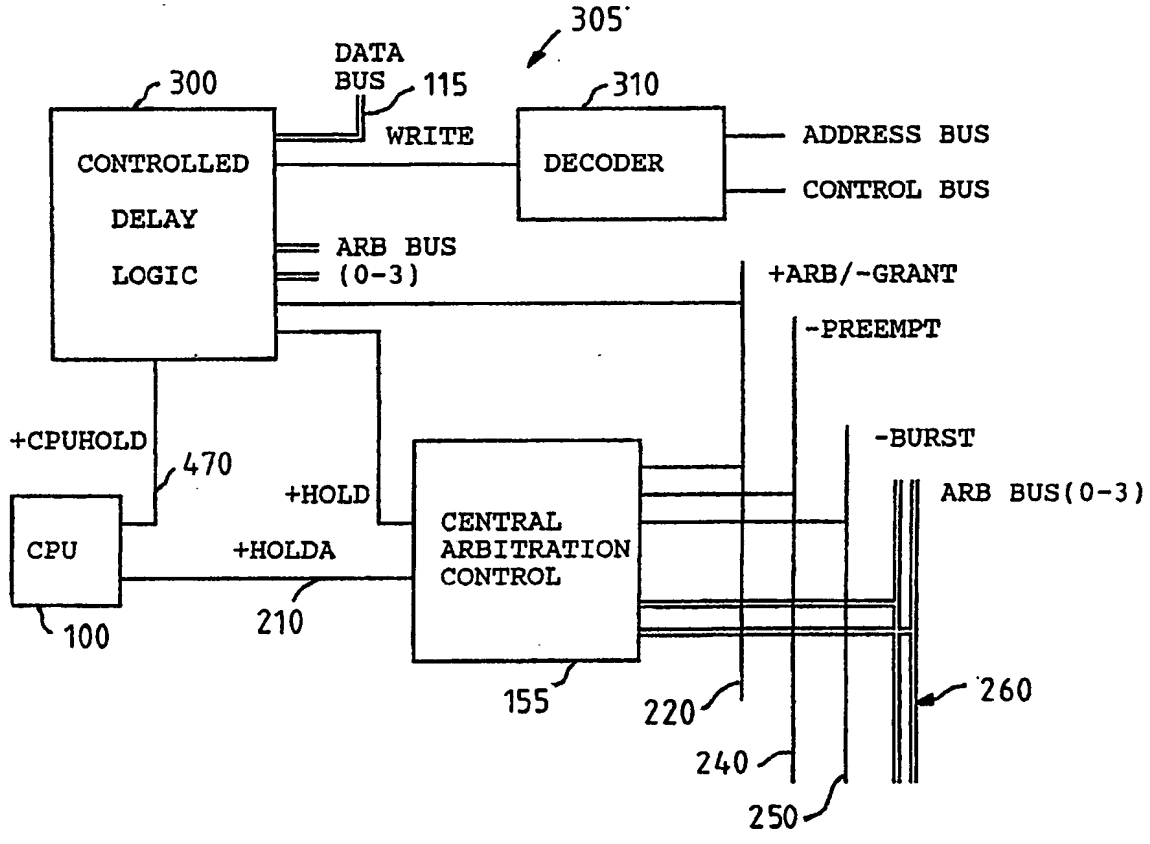

305
DATA
BUS
115
300
310
WRITE
CONTROLLED
DELAY
LOGIC
DECODER
ADDRESS BUS
CONTROL BUS
ARB BUS
(0-3)
+ARB/-GRANT
-PREEMPT
+CPUHOLD
470
-BURST
ARB BUS(0-3)
+HOLD
CPU
+HOLDA
CENTRAL
ARBITRATION
CONTROL
210
100
155
220
260
240
250

FIG. 3

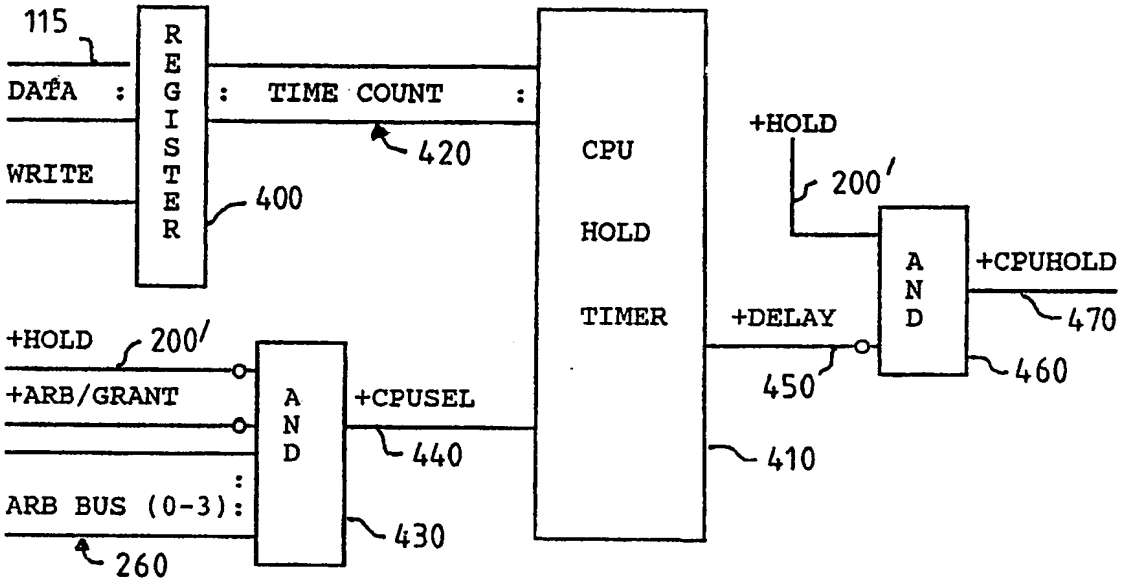
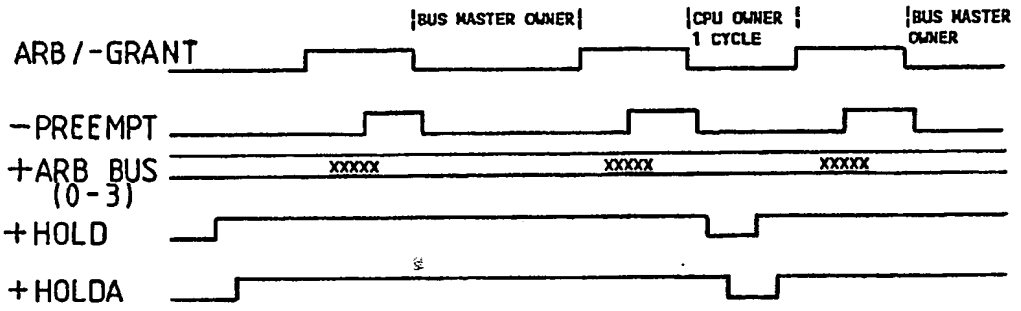

115
DATA
WRITE
REGISTER
400
TIME COUNT
420
CPU
HOLD
TIMER
410
+HOLD
200'
+ARB/GRANT
ARB BUS (0-3)
260
AND
+CPUSEL
440
430
+DELAY
450
+HOLD
200'
AND
+CPUHOLD
470
460

FIG. 4

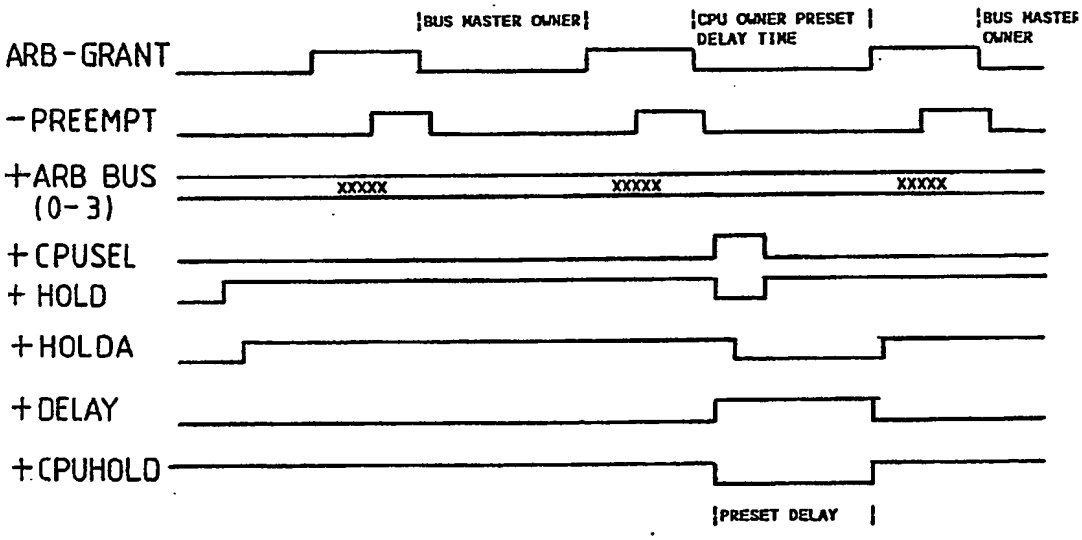
TIMING DIAGRAM FOR PRIOR ART




X ON ARBITRATION BUS INDICATES ARBITRATION TO IDENTIFY OWNER

FIG. 5

TIMING DIAGRAM ACCORDING TO INVENTION




X ON ARBITRATION BUS INDICATES ARBITRATION TO IDENTIFY OWNER

FIG. 6